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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/634,824	08/06/2003	Toshiyuki Arita	030905	6755

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EXAMINER	
BREWSTER, WILLIAM M	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 09/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/634,824	ARITA, TOSHIYUKI	
	Examiner	Art Unit	
	William M. Brewster	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *080603*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-9, 12, 13 are rejected under 35 U.S.C. 102(b) as being anticipated by Norio, Japanese Publication No. 07-045510, from the IDS, translation provided.

Norio anticipates a semiconductor apparatus fabrication method, comprising the steps of:

in fig. 1B, forming a resist pattern 2;

in fig. 1C, forming a film 4 whose heat-resistance temperature is higher than softening temperature of said resist pattern so as to cover said resist pattern;

in fig. 1D, heating said resist pattern at temperature higher than said softening temperature of the resist pattern and lower than said heat-resistance temperature of the film in a state where said film covers said resist pattern in order to cause reflow, p. 1, ¶ 6 ;

in fig. 1E, removing said film; and

patterning an underlayer of said resist pattern by using said resist pattern in which said reflow is caused as a mask, not shown, p. 2, ¶ 11-12;

limitations from claim 2, the semiconductor apparatus fabrication method as claimed in claim 1, wherein said film is an organic film whose softening temperature, which serves as said heat-resistance temperature, is higher than said softening temperature of the resist pattern, p. 1, ¶ 6;

limitations from claim 3, the semiconductor apparatus fabrication method as claimed in claim 2, wherein said organic film is soluble in one of an organic solvent and water, pp. 1-2, ¶ 7;

limitations from claim 4, the semiconductor apparatus fabrication method as claimed in claim 3, wherein said organic film is selected from a group of polyacrylic acid, polyvinylacetal, polyvinylpyrrolidone, polyvinylalcohol, polyethyleneimine, polyethyleneoxide, styrene- (anhydrous) maleic acid copolymer, methylvinylether- (anhydrous) maleic acid copolymer, polyvinyl amine resin, polyallylamine, water soluble oxazoline group containing resin, water soluble melamine resin, water soluble urea resin, alkyd resin, and sulfonamide resin, p. 2, ¶ 10;

limitations from claim 5, the semiconductor apparatus 25 fabrication method as claimed in claim 3, wherein said organic film is selected from a group of polyimide, polyacetal, polybutylene terephthalate, polyethylene terephthalate, syndiotactic polystyrene, poly phenylene sulfide, polyetherether ketone, liquid crystal polymer, fluorine resin, polyethernitrile, polycarbonate, modified poly phenyleneether, polysulfone, polyethersulfone, polyacrylate, polyalylate, polyamide-imide, thermoplastic polyimide, phenol resin, urea resin, melamine

resin, alkyd resin, unsaturated polyester, epoxy resin, diallyl phthalate resin, silicon resin, and polyurethane, pp. 1-2, ¶ 7;

limitations from claim 6, in fig. 1C, the semiconductor apparatus fabrication method as claimed in claim 2, wherein said step of forming the film includes a coating step;

limitations from claim 7, the semiconductor apparatus fabrication method as claimed in claim 1, further comprising a step of accreting a release agent on a surface of said resist pattern after the step of forming the resist pattern and before the step of forming the film, p. 2, ¶ 10-11, using alcohol;

limitations from claim 8, the semiconductor apparatus fabrication method as claimed in claim 1, wherein said film is an inorganic film whose melting point, which serves as said heat-resistance temperature, is higher than said softening temperature of the resist pattern, p. 1, ¶ 6;

limitations from claim 9, the semiconductor apparatus fabrication method as claimed in claim 8, wherein said inorganic film is formed in accordance with one of a coating method, a sputtering method and a plasma CVD method: coating, , p. 1, ¶ 6;

limitations from claim 12, the semiconductor apparatus fabrication method as claimed in claim 1, wherein said resist pattern is formed as a convex pattern on said underlayer, figs. 1C-E;

limitations from claim 13, the semiconductor apparatus fabrication method as claimed in claim wherein said resist pattern has an aperture for exposing said underlayer, figs. 1C-E.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Norio as applied to claims 1-9, 12, 13 above, and further in view of Wolf, Stanley Wolf Ph.D. and Richard N. Tauber Ph.D. in Silicon Processing for the VLSI Era, Volume 1: Process Technology, Lattice Press, 1986, pp. 365-8.

Norio states in pp. 1-2, ¶ 7 the use of inorganic film as a film to cover the resist, but does not specify what type, but Wolf does use metal. Wolf, below Deposition of Alloy Film f pp. 367 uses metal wherein said film is a metal film whose melting point, which serves as said heat-resistance temperature, is higher than said softening temperature of the resist pattern; wherein said metal film is formed in accordance with a sputtering method. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to recognize that combining Wolf's process with Norio's invention would have been beneficial because the invention as metal is inexpensive and commonly used in wafer fabrication.

Claims 14-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Norio as applied to claims 1-9, 12, 13 above, and further in view of Oiwa, Japanese Publication No. 2001015479 A.

Norio does not specify using multiple layers on the substrate to etch, but Oiwa does. Oiwa teaches in figs. 1A-E

limitations from claim 14, the semiconductor apparatus

fabrication method as claimed in claim 1, wherein said underlayer is a semiconductor film 12;

limitations from claim 15, the semiconductor apparatus fabrication method as claimed in claim 1, wherein said underlayer is an inorganic insulation film 14;

limitations from claim 16, the semiconductor apparatus fabrication method as claimed in claim 1, wherein said underlayer is an organic insulation film 15;

limitations from claim 17, the semiconductor apparatus fabrication method as claimed in claim 1, wherein said underlayer retains an antireflection film 15;

limitations from claim 18, in fig. 1C, the semiconductor apparatus fabrication method as claimed in claim further comprising step of patterning a film under said underlayer by using said underlayer as a mask, 13-14, all described in the solution.

Oiwa gives motivation in PROBLEM TO BE SOLVED. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to recognize that combining Oiwa's process with Noria's invention would have been

beneficial because the invention allows for manufacturing a semiconductor element without etching a silicon substrate when eliminating a mask layer.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to William M. Brewster whose telephone number is 571-272-1854. The examiner can normally be reached on Full Time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

William M. Brewster

16 September 2004
WB